

Building a Direct Digital Synthesis VFO

This DDS-based VFO requires few parts and is a good starting DDS project.

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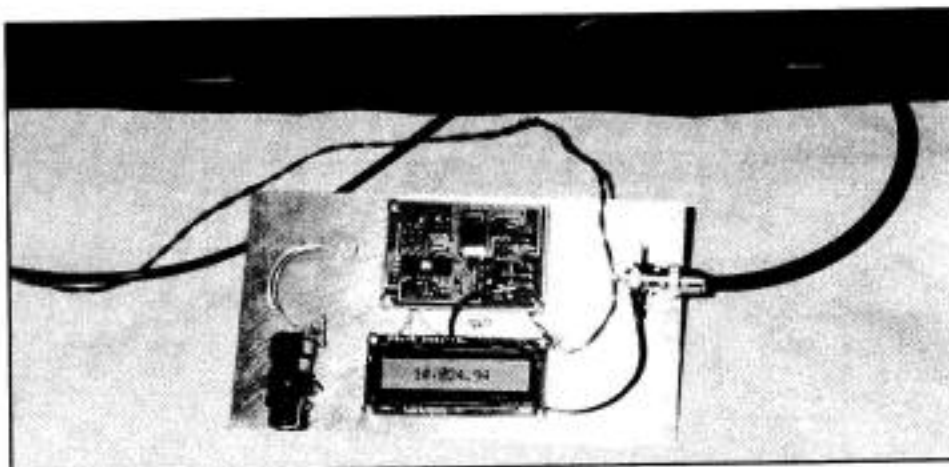
Since direct digital synthesis (DDS) was invented¹ in 1970, it has become more and more prevalent in the communications world—including Amateur Radio. Some interesting articles have been published in amateur-radio magazines explaining how DDS works.^{2,3} However, if you have an interest in building something with DDS, finding a related construction project is a problem.

The purpose of this project was to try out DDS by building a DDS-based VFO. The project was deliberately kept as basic as I could make it. It was very tempting to add a few bells and whistles since DDS has many capa-

¹Notes appear on page 7.

bilities, but there were enough problems to solve as it was. Of course, the first problem was to get hold of a DDS integrated circuit. Some Web surfing

revealed that a number of companies are supplying DDS chips or hybrids. These range from commodity CMOS devices that have clock rates up to



The DDS VFO. The rotary shaft encoder is at the lower left.

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125 MHz to specialty GaAs devices with clock rates over 1 GHz. Corresponding prices range from about ten dollars (in quantity) to several thousand dollars. Several of these companies also supply evaluation boards for their devices. These would be fine for a technical evaluation, but I wanted to apply DDS to an amateur-radio project. I decided to base the VFO on a CMOS DDS chip, the AD9850, that was announced by Analog Devices Inc in April of 1996. An AD9850 and a few other components were used to build a VFO that can tune from 100 kHz to 20 MHz in 10-Hz steps.

Project Description

DDS chips such as the AD9850 convert a reference oscillator input into a sine wave output at a frequency selected by the user. Basically, this project provides a mechanism to set the AD9850 for a desired frequency. See Fig 1 for a block diagram of the project. A complete schematic is shown in Fig 2. The rotary shaft encoder shown is for dialing in a frequency. A microcontroller monitors the outputs from the rotary encoder. The microcontroller then translates the rotary encoder signals into frequency control data, which is loaded into the DDS chip. Likewise, the microcontroller translates the selected frequency into data for display on the liquid-crystal display. The reference oscillator provides a digital clock to the DDS chip. The purpose of the low-pass filter is to smooth the digitized sine wave output of the DDS chip.

Microcontroller

A quick look at the schematic shows it doesn't take many parts to use the AD9850. The control program stored on the microcontroller contains most of the complexity involved with this

project. The nice thing about programs is that they are easy to replicate. A complete listing of the source code for this project is available at <ftp://ftp.arri.org/pub/qex>. The microcontroller is a low-cost 8-bit device from Microchip Technology.⁴ It has an on-chip EPROM for storage of 512 instruction words and 24 bytes of RAM for data storage. The program for this project uses 474 instructions and requires 23 bytes of RAM, so adding any features would require moving up the microcontroller product line to a device with more memory. The EPROM programmer used to load the code onto the microcontroller is from Parallax. This programmer comes with an assembler and debugging program. The manual for the programmer contains several sample projects that were very helpful in getting started. The debugger program also proved to be invaluable. I also put an EPROM eraser to good use.

The DDS Chip

The AD9850 is a complete DDS chip. It contains a 32-bit phase accumulator, a 14-bit look up table and a 10-bit digital-to-analog converter (DAC). It can be clocked at 125 MHz to produce a 41-MHz sine-wave output. The spurious-free dynamic range is greater than 50 dB at 40 MHz with a 125-MHz reference clock. A complete data sheet for the AD9850 can be downloaded from the Analog Devices web site at <http://www.analog.com/pdf/ad9850.pdf>.

The frequency control word for the AD9850 can be loaded byte-wide or serially. The serial mode is slower but is used in this project to minimize the number of output pins required on the microcontroller. Serial mode is selected as the default by wiring pin 2 of the AD9850 to ground while pins 3

and 4 are wired to the supply voltage. Pin 25 is the serial data input, and pin 7 is the data write clock. After shifting in 40 data bits, pin 8 is used to transfer the data from the chip's input register to the DDS core. The 40 bits are a 32-bit frequency control word, 3 control bits and 5 phase-modulation bits.

The AD9850 data sheet gives Eq 1 for calculating the required control word. In order to minimize program size, the actual calculation uses the algorithm shown in Eq 2. This algorithm has some round-off error, but the error is less than 1 Hz, which is small enough to ignore in this application.

$$F_{out} = (\Delta Phase \times ClkIn) / 2^{32} \quad \text{Eq 1}$$

Where: $\Delta Phase$ = value of the 32-bit tuning word, $ClkIn$ = reference clock frequency in MHz, and F_{out} = frequency of the output signal in MHz.

$$\Delta Phase = \sum_n LCD_Digit \times Digit_Weight$$

Eq 2

Where: $\Delta Phase$ is the control word sent to the AD9850, n is the range of 1 to 7, LCD_Digit is a one of the seven digits being display on the LCD, and $Digit_Weight$ is a precalculated value given in Table 1.

The AD9850 DAC output is a differential current on pins 20 and 21. A resistor placed from pin 12 to ground determines the full-scale output current for the DAC as given in Eq 3. The current equation is valid provided the voltage across the DAC output pins is less than 1.5 V. Setting the resistor to 3.92 k Ω yields a DAC current of about 10.2 mA. With the parallel load of the filter terminator and an external 50- Ω load, this current results in a voltage swing of about 250-mV peak-to-peak.

$$I_{out} = 32(1.248V / R) \quad \text{Eq 3}$$

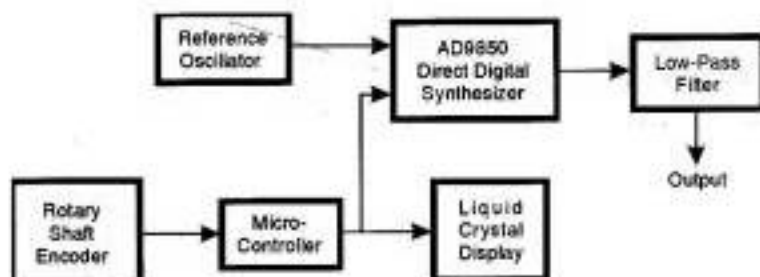


Fig 1—DDS VFO Block Diagram.



The AD9850 DDS chip is really small.

Rotary Shaft Encoder

The shaft encoder is optically coupled and has 32 detents. It has two digital output pins that cycle through a 00, 01, 11, 10 sequence as the shaft turns clockwise. Turning the shaft counterclockwise reverses the sequence. The control program monitors the shaft encoder outputs and decodes them to determine which way the shaft turned. At power-on reset the initial value of the VFO is 10 MHz. Each change of the encoder output causes the program to

increment or decrement the LCD frequency display, followed by the calculation of a new frequency control word that is sent to the DDS chip.

The control program also counts the time elapsed between encoder output changes and will make bigger or smaller frequency steps depending on how fast the shaft is being turned. The particular rotary encoder shown in the schematic also has a built-in push-button switch. Turning the shaft with the switch closed causes the control

program to change the frequency in 100-kHz steps. The combination of speed-controlled steps and 100-kHz steps allows rapid tuning across the VFO range. If there were only 10-Hz steps it would take 62,000 revolutions of the tuning knob to cover the VFO tuning range!

Liquid-Crystal Display

A wide variety of low-cost liquid-crystal displays are available, with different digit sizes or with back-

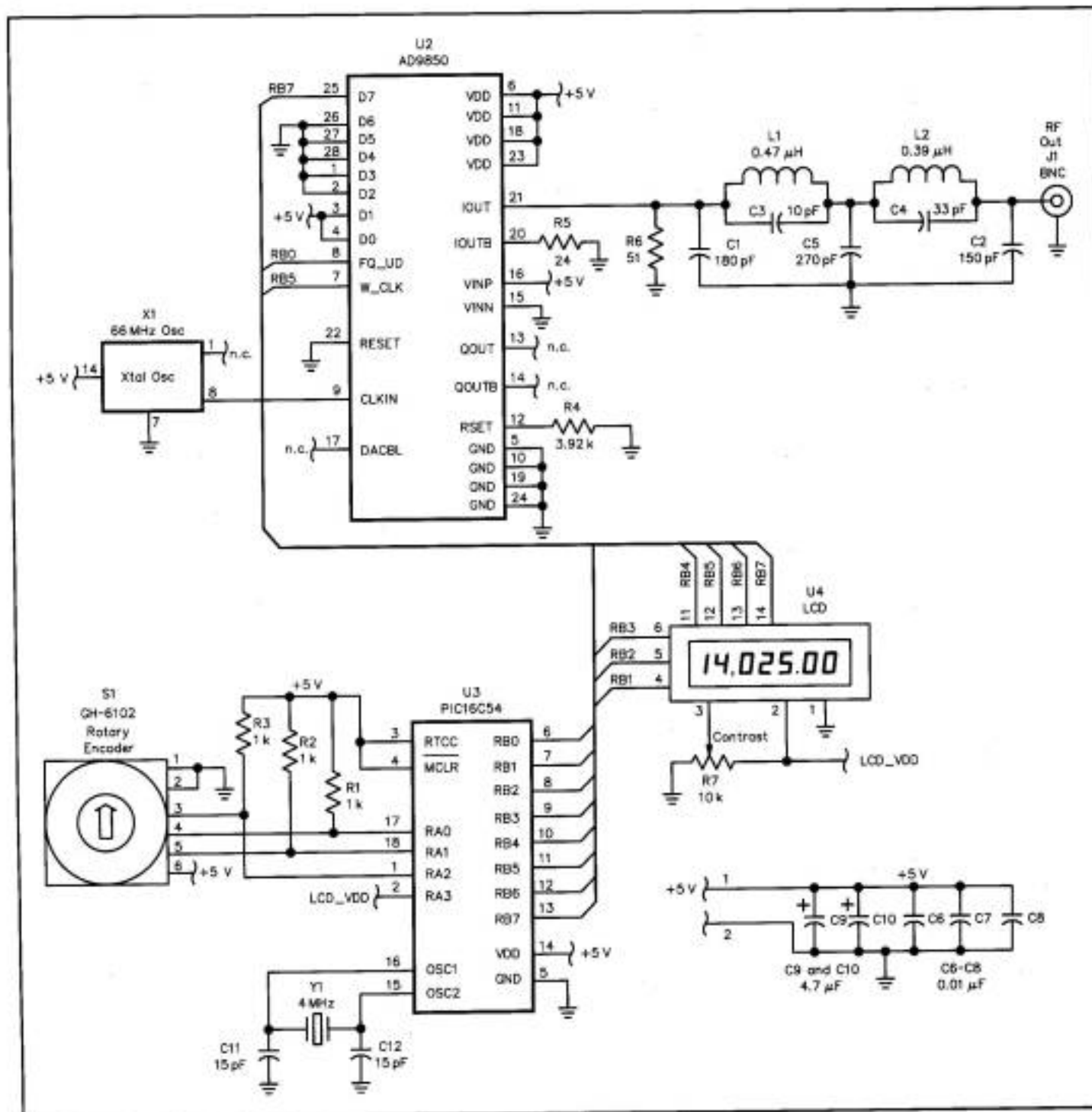


Fig 2—DDS VFO Schematic.

lighting. Fortunately, most of them use a common method of accepting data and control information. The control program assumes an LCD having a 16 by 1 display format. At power-on, commands are sent to the LCD that configure it for four data input bits instead of the normal 8-bit data mode. This minimizes the number of microcontroller pins required.

On the schematic, note that power for the LCD is being supplied from an output pin on the microcontroller. The reason for this is that the LCD was fussy about the turn-on time of the supply voltage and would not always reset properly. Using the microcontroller output pin for LCD power allows consistent power-on resets. Potentiometer R7 adjusts the LCD contrast.

Reference Oscillator

The reference oscillator is a standard clock oscillator module. The accuracy of the reference oscillator directly determines the VFO output accuracy. If the reference oscillator

has a 100-ppm tolerance, so does the output. Clock oscillator modules up to 66.666 MHz are readily available. For many vendors, higher frequencies are special order items. Choice of a reference frequency will depend on the application. Changing the reference frequency requires updating the control program values in Table 1. One factor in the choice of reference frequency might be the locations of spurs. All DDS systems will have low-level spurious outputs.⁵ The frequency of these spurs is very predictable. They are related to the reference clock frequency and harmonics of the output frequency.

Low-Pass Filter

The output of the DDS chip is a digitized or sampled sine wave. Such a wave shape has strong frequency components at the reference clock frequency plus or minus the output frequency. Filtering out these components produces a clean sine wave. For this project, with a reference clock near 66 MHz and a maximum output

frequency of 20 MHz, the low-pass filter must cut off frequencies above 46 MHz while passing frequencies below 20 MHz. The fifth-order elliptic low-pass filter⁶ shown in the schematic has 55 dB or greater attenuation at frequencies above 46 MHz. The filter requires a 50- Ω termination.

The calculated passband ripple of the filter is about 1 dB. However, a more significant amplitude variation can occur as the output frequency increases. As the output frequency goes higher, the digitized sine wave is constructed from fewer samples per cycle. At the DAC output pins, the wave shape begins to look less and less like a sine wave. As this happens the spurious frequency components constitute a larger portion of the total output power; meanwhile the desired output component is less.

Construction

A drawback to the AD9850, from a home-builder's point of view, is the package. The device is in a 28-lead SSOP, (shrink small outline package).

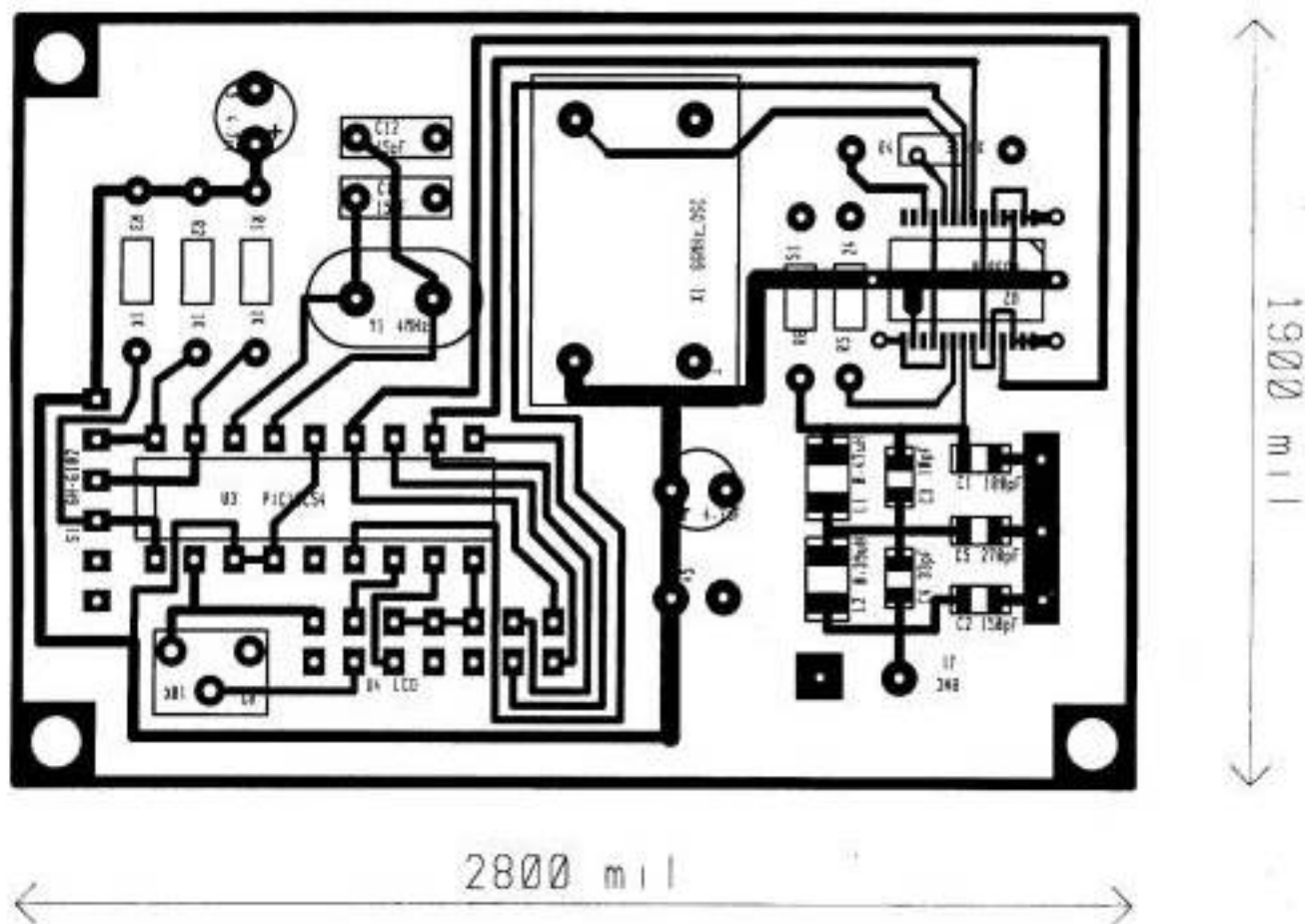


Fig 3—Component Layout.

The word for this package is tiny. The small size and close lead spacing made construction a challenge. A printed-circuit board is necessary. The use of surface-mount packages seems to be standard practice for suppliers of DDS chips. Some use leadless chip carriers, others use quad flat packs or small outline formats. Although the packages vary, experimenting with DDS means dealing with small packages.

The circuit board for the project was made with the use of iron-on transfer paper.⁷ The layout was done using a program called *WinBoard*.⁸ Fig 3 shows the layout that I used. One word of caution: this layout isn't necessarily an example of good layout practices. Simplifying board fabrication was the goal. The wiring around the DDS chip is very tight. I used a 600-dpi laser printer to print the pad patterns for this chip.

The board is double-sided, but only the component side is etched; the back side is a solid ground plane. Clearance on the ground side of vias was etched manually with a small drill bit. Eyelets were placed in the vias under the crystals. Decoupling caps for the DDS chip and clock module were placed on the ground side.

After making the board, the next challenge was getting the DDS chip soldered in place. With a 25-mil lead pitch, unintended solder bridges form between pins as if by magic. In a commercial environment the method for mounting such chips is to put a solder paste on the circuit board pads through a precisely made silk screen. The chips are positioned with a pick-and-place machine, then the whole board is sent through a heating chamber to reflow the solder paste. Lacking such equipment, I used a small soldering iron, some 25-gauge solder and a magnifying glass. There may be a better way, but at least one way to put the chip down is to tack it at one corner. Check and adjust the pin-to-pad alignment until it is right then tack the other corners. Once that's done just solder the pins, letting bridges form where they may, then use copper desoldering braid to wick the pins clean. The pads for the DDS chip demand careful use of the soldering iron. Too much heat or pressure will tear these off the board.

Conclusion

While this project was probably overkill as the VFO for a basic radio, it was a great excuse to try out new

Table 1: Digit Weights for a 66.666-MHz Reference Clock

LCD_Digit	Digit_Weight (in hex)
10's	284
100's	192A
1k	FBA9
10k	9D49B
100k	624E13
1M	3D70CC1
10M	26667F90

Table 2: Parts List

Reference	Value/Description	Part Number
C1	180-pF chip capacitor	PCC181CGCT-ND
C2	150-pF chip capacitor	PCC151CGCT-ND
C3	10-pF chip capacitor	PCC100CNCT-ND
C4	33-pF chip capacitor	PCC330CGCT-ND
C5	270-pF chip capacitor	PCC271CGCT-ND
C6,C7,C8	0.01- μ F chip capacitor	PCC103BNCT-ND
C9,C10	4.7- μ F tantalum	P2011-ND
C11,C12	15-pF ceramic disk	P4014A-ND
L1	0.47- μ H chip inductor	DN10471CT-ND
L2	0.39- μ H chip inductor	DN10391CT-ND
R1,R2,R3	1-k Ω , 5%, 1/4 W	1KQBK-ND
R4	3.92-k Ω , 1%, 1/4 W	3.92KXBK-ND
R5	24- Ω , 5%, 1/4 W	24QBK-ND
R6	51- Ω , 5%, 1/4 W	51QBK-ND
R7	10-k Ω potentiometer	31G14-ND
U2	DDS chip	AD9850BRS
U3	Microcontroller (not-programmed)	PIC16C54/JW-ND
LCD1	16x1 liquid crystal display	73-1016-ND
S1	Rotary shaft encoder	GH6102-ND
Y1	4-MHz crystal	CTX006-ND
X1	66.666-MHz crystal oscillator	XC228-ND

Except for the AD9850 DDS chip, all these parts are known to be available from Digi-Key. Any equivalent parts can be used. A list of distributors for the AD9850 is available from Analog Devices. However, at the time of writing only FAI Electronics Corporation, (800-707-6040) had AD9850s in stock. Retail price was \$21.00. For convenience, the Digi-Key stock numbers are shown. The EPROM programmer by Parallax is available from Digi-Key as is an EPROM eraser from the Walling Co.

things. DDS has significant advantages in many applications and its use will become increasingly common. There are a number of modulation techniques that can be used with DDS. Some CMOS chips with modulation capabilities are available. DDS can also be combined with phase-locked loop circuits to produce some interesting systems. Lots of possibilities!

Notes

¹IEEE Transactions on Audio and Electroacoustics, Vol. AU-19, No. 1, March 1971, pp 48-56.

²Bergeron, "Direct Digital Synthesis: An Introduction," *Communications Quarterly*, Summer 1993, p 13.

³Cahn, "Direct Digital Synthesis—An Intuitive Introduction," *QST*, August 1994, p 30.

⁴Data sheets are available at <http://www.microchip.com/>.

⁵Bar-Giora Goldberg, *Digital Techniques in Frequency Synthesis*, pp 107-118.

⁶Stefan Niewiadomski, *Filter Handbook: A Practical Design Guide*, Chapter 2.

⁷For more information on this process see the web site at <http://www.dynaart.com/>.

⁸A demo version of this program is available at <http://www.ivex.com/>. □